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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,411	07/30/2003	Tony Mule	62020-1220	9009
24504	7590	08/08/2005	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP			LEPISTO, RYAN A	
100 GALLERIA PARKWAY, NW				
STE 1750			ART UNIT	PAPER NUMBER
ATLANTA, GA 30339-5948			2883	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,411	MULE ET AL.	
Examiner	Art Unit		
Ryan Lepisto	2883		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 June 2005.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 11-38 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 11-18, 25-27 and 38 is/are allowed.

6) Claim(s) 19-22, 28, 30-33 and 35-37 is/are rejected.

7) Claim(s) 23, 24, 29 and 34 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 30 July 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. _____.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 28, 30-33 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Ding (US 6,351,576 B1).** Ding teaches a device for microelectronic optical clock distribution (abstract) comprising an integrated circuit device (Fig. 2 202), a reflecting cladding (Fig. 2, 260, it reflects light traveling through the core region, implying a lower index of refraction and it surrounds and is disposed on the core region, so it can be defined as a cladding) disposed on the back of the integrated circuit substrate (208), a waveguide (Fig. 3, 264 or Fig. 5, 564 that is shown as structure 222 in Fig. 2) with a light guiding core region (region where beam (268) travels) disposed on the P-epi cladding layer (110) wherein the core region (shown in Fig. 5, part of 564, 584) includes a vertical-to-horizontal diffractive metal mirror (DMM, diffractive metal mirror being an art equivalent to a diffractive grating) (522) (with as is shown in Fig. 2, a stepped or surface-relief structure) for distributing (and multiplexing, therefore the mirrors are diffractive multiplexing mirrors) an optical clock signal from a source through the entire

core layers to a horizontal-to-horizontal DMM (578) for distributing an optical clock signal in two separate (plurality of) directions through the core layer to two horizontal-to-verticals DMMs (566) for distributing an optical clock signal from a source to revivers (518) (column 9 lines 1-22), a second reflecting cladding (Fig. 2, 262, it reflects light traveling through the core region, implying a lower index of refraction and it surrounds the core region, so it can be defined as a cladding) adjacent to the core region, a chip-level detector (218) on the integrated circuit device (202), a chip-level dielectric via (220) (column 5 lines 8-10), a chip-level optical source (248, from a fiber, not shown, column 8 lines 5-6) and a substrate (implying, printed wiring board) (208).

Ding further teaches the method and means of forming the structure (Fig. 9) comprising providing the substrate (a cladding (210) is a part) (900), disposing the core region on the substrate (cladding (210) included) and the diffractive DMMs (either simultaneously (920) or separately (930 to 910)) wherein the cladding layers (260, 262) are fabricated during metallization (etching is a widely used process) on the core region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 19-22 and 35-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding as applied to claims 28, 30-33 and 37 above, and further in view of **Brophy et al (US 2003/0034538 A1)** (Brophy).

Ding teaches the optical clock distribution device described above.

Ding does not teach expressly creating the diffractive (mirrors or gratings) in cladding layers.

Brophy teaches a device for optical clock signals (paragraph 0150) comprising waveguide core layer (Fig. 44, 1206) and cladding layer (1204) adjacent the core including a grating structure (1203) etched in it. Brophy teaches a further embodiment with core (Fig. 45, 1238), a first cladding (1236) and a second cladding (1234) with a grating structure (1233) etched in it.

Ding and Brophy are analogous art because they are from the same field of endeavor, optical clock distribution devices using diffractive elements in or around waveguide core and claddings to route a signal.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to create diffractive elements in cladding layers as is taught by Brophy with it being obvious in the device as taught by Ding to have additional claddings where the diffractive mirrors (or gratings) may be produced, separate the waveguide core region.

The motivation for doing so would have been to be able to tune the indices of refraction of the gratings more easily by being able to use widely used manufacture techniques with cladding regions (Brophy, paragraphs 0172, 0176, 0178-0179)

Allowable Subject Matter

3. **Claims 11-18, 25-27 and 38** are allowed.

Claims 23-24, 29 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

With regard to claims 11, 25 and 38: These claims are allowable over the prior art of record because the latter, either alone or in combination, does not disclose nor render obvious a structure for optical clock distribution with the particular combination of the following; a core layer with at least one vertical-to-horizontal input diffraction grating configured to diffract the clock signal from a vertical plane to a horizontal one, at least one horizontal-to-horizontal diffraction grating configured to diffract the clock signal through a horizontal plane and at least one horizontal-to-vertical output diffraction grating configured to diffract the clock signal from a horizontal plane to a vertical one wherein each grating diffracts the clock signal in a plurality of directions and so the signal is uniformly distributed through the core layer, or the same gratings being disposed on a first write-wavelength vertical reflection absorption cladding which is disposed on the back side of an integrated circuit device wherein a signal is diffracted from the vertical-to-horizontal to the horizontal-to-horizontal to the horizontal-to-vertical grating in that order where at least one of the gratings diffracts the signal in a plurality of

directions and uniformly through the core together with a chip-level dielectric filled through-wafer optical via, in combination with the rest of the claimed limitations.

With regard to claims 23, 29 and 34: These claims would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the latter, either alone or in combination, does not disclose nor render obvious a vertical reflection absorption layer adjacent to or on a second cladding layer or etching away a portion of the core at the edges of the substrate and replacing it with a horizontal reflection absorption layer, in combination with the rest of the parent claimed limitations.

With regard to claim 24: This claim would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims because it depends from a claim with allowable subject matter.

With regard to claims 12-18 and 26-27: These claims are allowable over the prior art of record because they depend from allowable claims.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection because of applicant's amended claims.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Lepisto whose telephone number is (571) 272-1946. The examiner can normally be reached on M-F 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2883

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RAV

Ryan Lepisto

Art Unit 2883

Date: 8/9/05

Frank L. Font

Frank Font

Supervisory Patent Examiner

Technology Center 2800